IN THE CLAIMS

Please amend the claims as follows:

Claims 1-22 (Canceled).

Claim 23 (Currently Amended): A non-volatile semiconductor memory device, comprising:

a plurality of memory cell units comprising at least one memory cell having a laminated gate structure of a charge accumulation layer and a control gate layer formed above ~~on~~ a semiconductor substrate, with ~~above~~ a gate insulation film provided between the laminated gate structure and the semiconductor substrate; and

a plurality of selection gate transistors each having a gate electrode formed on ~~above~~ the gate insulation film and source/drain diffusion layers, one of which is connected to each memory cell unit and the other of which is electrically connected to a bit line or a source line,

wherein the plurality of selection gate transistors include a pair of ~~first~~ selection gate transistors disposed in confrontation with each other across a contact portion connected to the bit line or to the source line and having substantially the same structure; and

channel regions of the pair of selection gate transistors have a same impurity concentration in a gate length direction at a depth equal from the boundary between the semiconductor substrate and the gate insulation film as well as a concentration distribution of impurity in the channel regions of the pair of selection gate transistors is different from that of a channel region of the memory cell, and

an impurity distribution width in a depth direction of the channel region of each of the pair of ~~first~~ selection gate transistors is narrower than that of the channel region of the memory cell.

Claims 24-52 (Canceled).